The SuperPix0 Small-Pitch Hybrid Pixel Detector with Fast Sparsified Digital Readout: Beam Test Results

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Abstract

A prototype hybrid pixel detector with 50×50 μm^2 pixels, 200 μm thick sensor and sparsified digital readout has been tested with a 120 GeV pion beam at the SPS H6 beam line at CERN. Both effciency and resolution have been measured as a function of the discriminator threshold and the angle of incidence of the impinging particles. The capabilities of the custom data-push readout architecture have been tested as well. The viability of this technology for the full-luminosity upgrade of the layer 0 of the SuperB vertex detector is discussed.

Keywords: CMOS pixels, Charged particle tracking, Hybrid pixel detector, Data-push readout

1. Introduction

The SuperB B-Factory [**?**], a new concept asymmetric e^+e^- collider dedicated to heavy-flavour physics and expected to deliver unprecedented luminosities in excess of 10^{36} cm^{-2}s^{-1}, has been funded by the Italian Ministry of

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Education, University and Research in the framework of the 2011-2013 National Research Plan (Dec. 24 2010). Its reduced center-of-mass boost with respect to previous B-Factories (BaBar [?] and Belle [?]) asks for a factor two improvement on typical vertex resolutions to fully exploit the accelerator potential for new-physics discoveries. In addition, the high luminosity and large backgrounds expected at SuperB determine stringent requirements in terms of granularity, time resolution and radiation hardness of all subdetectors and in particular, the vertex detector which is the closest to the interaction point.

The design of the SuperB Silicon Vertex Tracker follows the model of the BaBar SVT [?] but comprises both an extended coverage and an additional innermost layer, called layer 0, located at about 1.5 cm radius from the beam line. The layer 0 should offer a low material budget to minimize multiple scattering so as to meet the requirements on vertex resolution, and must be provided with a high-speed readout to minimize the acquisition dead-time. Intense R&D studies on various emerging technologies have been carried out to address further requirements such as a small pitch to guarantee a hit resolution at the level of 10 μm and to limit detector occupancy, the capability to withstand background hit-rates up to a few tens of MHz/cm^2, large signal-to-noise ratio and low power dissipation. Standard high resistivity silicon detectors with short strips (striplets) will be used for the layer 0 during the first period of operation, when the luminosity will be gradually increased to reach the design value. In fact, striplets offer a reasonably low material budget (about 0.2-0.3 $\%X_0$ for 200-300 μm silicon thickness) together with the required hit resolution. However, the detector occupancy becomes unaffordable at background rates larger than 5 MHz/cm^2 as expected at full luminosity, and a detector replacement is already scheduled after the first period of running.

This paper is focused on a prototype hybrid pixel detector named SuperPix0 and designed by the VIPIX collaboration as a first iteration step aimed at the development of a device to be used for the layer 0 upgrade.

Hybrid pixel devices are a well established technology in HEP experiments. The fully depleted high-resistivity sensors and the read-out integrated circuits are built on different substrates and then connected via high density bump-bondings. Hybrid pixel sensors usually provide high signal-to-noise ratio, high radiation tolerance and 100% fill factor. Furthermore, this technology offers the possibility to implement advanced in-pixel electronics such as low-noise amplification, zero suppression and threshold tuning without the problem of cross-talk between the readout logic and the sensor. The relatively large amount of material they are made of represents a disadvantage in terms of probability of particle scattering, although a reduction of material budget may become possible with the latest technology improvements [**?**]. The main novelties of our approach is the sensor pitch size (50×50 μm^2) and thickness (200 μm) as well as the custom front end chip architecture providing a sparsified and data-driven read-out. A prototype readout chip with 4096 cells arranged in a 32×128 matrix was submitted for fabrication in standard 130 nm CMOS technology by STMicroelectronics. The sensor was fabricated by FBK-IRST and interconnected with the readout chip by IZM.

The paper is organized as follows:

2. The SuperPix0 Hybrid Detector

2.1. The High Resistivity Pixel Sensor

Pixel sensors are made from n-type, Float Zone, high-resistivity silicon wafers, with a thickness of 200 μm and a nominal resistivity larger than 10 kΩcm. Sensors are of the "n-on-n" type and were fabricated at FBK (Trento, Italy) with a double-sided technology [**?**]. N^+ pixels are arranged in a 2d array of 32×128 elements with a pitch of 50 μm in both X and Y directions, for a total active area size of 10.24 μm^2 . All around the pixels is a large n^+ guard ring extending up to the cut-line. The electrical isolation between neighboring n^+ pixels has

been obtained by means of a uniform p-spray implantation. A large p^+ diode is on the bias side: it has the same size as the active area and is surrounded by 6 floating rings. From electrical tests performed on wafers before bump-bonding (and connecting the sensors from the bias side only with a probe on the diode and a probe on the scribe line [**?**]), the total leakage current is about 1 nA, the depletion voltage is about 10 V, and the breakdown voltage in the order of 70 V, due to a relatively high p-spray dose. The pixel capacitance has also been estimated from measurements performed on a special test structure, and the resulting values are in the order of 50 fF (i.e. close to the capacitance contribution expected from the bumps).

2.2. The Front End Cell

The in-pixel analog electronics is made of a charge processor (shown in Fig. **??**) where the sensor charge signal is amplified and compared to a chip-wide preset threshold by a discriminator. The in-pixel digital logic, which follows the

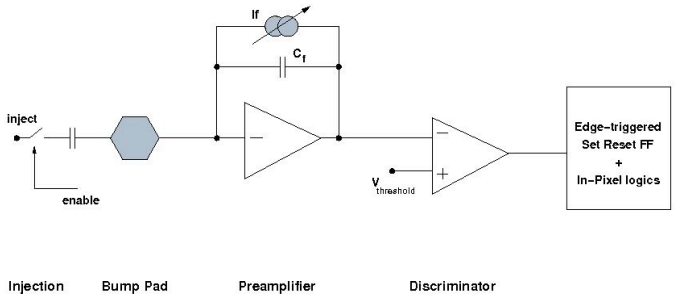

Figure 1: Block diagram of the analog front end electronics for the elementary cell of the SuperPix0 readout chip.

comparator, stores the hit in an edge-triggered set reset flip-flop and notifies the periphery readout logic of the hit. The charge sensitive amplifier uses a single-ended folded cascode topology, which is a common choice for low-voltage, high gain amplifiers. The 20 fF MOS feedback capacitor is discharged by a constant current which can be externally adjusted, giving an output pulse shape that is dependent upon the input charge. The peaking time increases with the collected

charge and is in the order of 100 ns for 16000 electrons injected. The charge collected in the detector pixel reaches the preamplifier input via the bump-bond connection. Alternatively, a calibration charge can be injected at the preamplifier input through a 10 fF internal injection capacitance so that threshold, noise and crosstalk measurements can be performed. The calibration voltage step is provided externally by a dedicated line. Channel selection is performed by means of a control section implemented in each pixel. This control block, which is a cell of a shift register, enables the injection of the charge through the calibration capacitance. Each pixel features a digital mask used to isolate single noisy channels. This mask is implemented in the readout logic. The input device (whose dimensions were chosen based on [**?**]) featuring an aspect ratio W/L=18/0.3 and a drain current of about 0.5 μA, is biased in the weak inversion region. A non-minimum length has been chosen to avoid short channel effects. The PMOS current source in the input branch has been sized to have a smaller transconductance than the input transistor. For a detector capacitance of 100 fF, an equivalent noise charge of 150 e^- rms was obtained from circuit simulations. The noise contribution arising from the leakage current can be neglected for the leakage current range considered in the simulations (0-2 pA). 2 pA corresponds to ten times the anticipated leakage current for the pixel sensor. An overall input referred threshold dispersion of 350 e- rms was computed from Monte-Carlo simulations. Since SuperPix0 is the first iteration step aimed at the development of a readout chip for small pitch hybrid pixel sensors, in this design only the main functionalities have been integrated in the pixel cell. Threshold dispersion is a crucial characteristic to be considered in order to meet the required specifications in terms of noise occupancy and efficiency. Therefore, circuits for in-pixel threshold fine-adjusting have to be implemented in the next version of the chip. The analog front end cell uses two power supplies. The analog supply (AVDD) is referenced to AGND, while the digital supply is referenced to DGND. Both supplies have a nominal operating value of 1.2 V. Since single-ended amplifiers are sensitive to voltage fluctuations on the supply lines, the charge preamplifier is connected to the AVDD. The threshold discrim-

inator and voltage references are connected to both the AVDD and AGND. The in-pixel digital logic is connected to the digital supply. The substrate of the transistors is connected to a separate net and merged to the analog ground at the border of the matrix. The SuperPix0 chip has been fabricated in a six metal level technology. Two levels of metal have been used to route the analog signals, two for the digital ones and two for distributing the analog and digital supplies. The supply lines, at the same time, shield the analog signals from the digital activity. For nominal bias conditions the power consumption is about 1.5 μW per channel. More details on the design of the analog front end chip can be found in the literature [**?**].

2.3. Digital Readout Architecture

The SuperPix0 digital readout architecture is an evolution of the one adopted for the APSEL4D chip [**?**] and was originally designed to read out matrices of 320×256 pixels and sustain rates of 100 MHz/cm^2 . The same macro-pixel (MP) structure as described in [**?**] has been adopted, but with a different MP shape: 2×8 pixel rectangles replace 4×4 pixel squares in order to minimize the matrix mean sweeping time (MST) in the presence of hit-clusters as expected in the data. A further parallelisation level is achieved by dividing the matrix in sub-matrices of 32×64 pixels and providing each sub-matrix with an independent readout and a local data buffer. A final output stage retrieves data from all the readout buffers and compresses them into a single data stream. Hits are extracted from the matrix in a time-ordered way, which was not the case with the APSEL4D chip and which allows avoiding to add time information to each hit, thus reducing the total amount of data to be transferred. Finally, a new hit encoding algorithm is used that includes a data compression for clustered hits; in this way the output data band-width is significantly reduced with a negligible increase of logic gates.

Each MP is connected to the peripheral readout through two private lines used to send a "hit" information when at least one of the pixels in the MP is

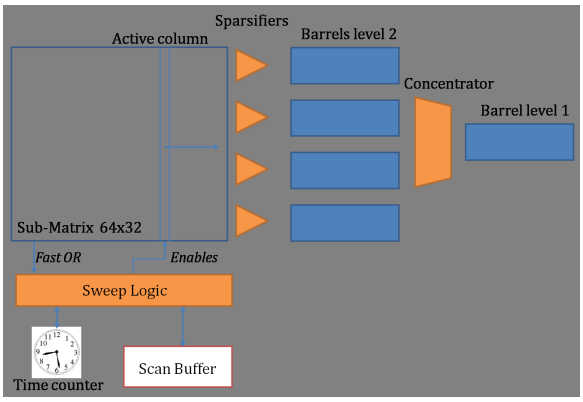

Figure 2: Schematics of the digital readout architecture.

fired and to receive a "freeze" signal to prevent all the pixels within the MP from accepting further hits until the readout has been completed. The peripheral readout includes a time counter (BCO) which is incremented at the frequency of a programmable clock defining the time resolution of the detector. Its value is used to provide a time-stamp to each event. Whenever the BCO counter is incremented, the MPs that have been hit during the previous time window are frozen and their hit-map is stored inside a FIFO together with the associated time stamp. The list of active MPs is then used to extract hits from the matrix in a time-ordered way. A 32-bit wide pixel data bus is shared by the rows and driven by the columns of the pixel matrix. For each BCO, the readout is performed only on the columns in the corresponding MP list, one column per readout-clock cycle (down to 6 ns) independently of the pixel occupancy. Only pixels belonging to the fired MP are enabled to drive the corresponding lines of the pixel data bus. When compared to a continuous sweep over the matrix columns as performed with the APSEL4D chip, this technique slightly increases the mean pixel dead-time. On the other hand, simulations demonstrated that the rectangular MP geometry results in an overall improvement of performance with respect to the APSEL architecture for any fixed number of hits.

A schematic of the perifery digital logic is shown in Fig **??**. As in the

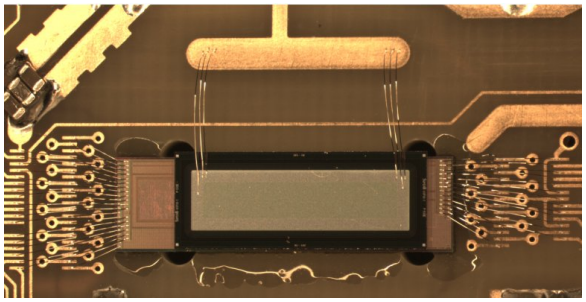

Figure 3: Photograph of the bump-bonded chip, the sensor matrix and the front end chip are visible as well as the bondings to the carrier.

APSEL4D chip, the pixel data are encoded by the sparsifier elements. They create a formatted list of all the hits found on the pixel data bus and write it into a dedicated memory element called barrel. This component is a FIFO memory with multiple write ports (one for each word in the list) and a conventional single output port. A data concentrator controls the flux of data preserving the time-sorting of the hits.

Monte Carlo simulations have been performed on this architecture scaled to a 320×256 matrix in order to evaluate its performance. We measured efficiencies close to 98.5% running with a 60 MHz readout-clock (200 MHz on the output bus) and starting from the assumption of a 100 MHz/cm^2 hit rate. Whilst keeping in mind that the target time resolution for this architecture is 1 μs, an efficiency drop is observed with BCO lengths below 400 ns.

2.4. Chip Characterization

Five chip matrices have been characterized in terms of noise, threshold dispersion and gain in various laboratory tests before the final trial on beam. The response of the sensors was analysed as well. A photograph of one of the front end chips connected by bump-bonding to the high resistivity pixel sensor matrix of 200 μm thickness is shown in Fig. **??**. The first laboratory checks identified a marginal problem in the readout architecture that was investigated with dedicated studies. A particular data acquisition configuration allowed the problem

chip	thr. disp. (e^-)	ENC (e^-)	gain (mV/fC)
12	460 ± 30	71 ± 1	37.3
19	500 ± 30	85 ± 1	38.7
53	520 ± 30	77 ± 1	38.6
54	500 ± 30	77 ± 1	39.2
55	580 ± 30	77 ± 1	36.9

Table 1: Lab characterization of the 5 chips tested during the test-beam.

to be overcome, although the measurements were limited to 3% of the pixels of the matrix for each run. Time constraints allowed the characterization of the front end electronics of about 10-20% of the pixels in each matrix, depending on the chip. The absolute calibration of the gain of the chip matrix was performed by using the internal calibration circuit described in **??**, which allowed the injection of charges from 0 to 12 fC in each preamplifier. An average gain of 38 mV/fC was measured with a typical dispersion of about 6% inside the examined piece of matrix.

Noise measurements and an evaluation of the threshold dispersion were performed by measuring the hit rate as a function of the discriminator threshold. With a fit to the turn-on curve we obtain a pixel average equivalent noise charge (ENC) of about 77 e^- with 15% dispersion inside the matrix, and a threshold dispersion of about 500 e^-, which motivated the project of a threshold tuning circuit at pixel level for the next submission. Threshold dispersion, ENC and gain values for each of the 5 chips characterized in the laboratory are reported in Table **??**.

Both beta (^{90}Sr) and gamma (Am) radioactive sources were used in order to test the sensor response and the interconnections between the pixel electronics and the sensor. The hit rate as seen from the sensor matrix when exposed to ^{90}Sr is shown in Fig.. **??**. The illumination of the matrix is not uniform due to the collimation of the source. The two blank columns are due to a known

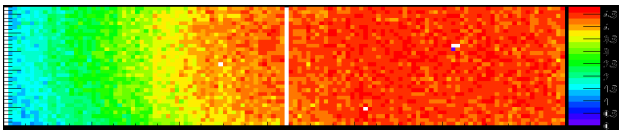

Figure 4: Hit rate (Hz) measured with chip 19 exposed to a ^{90}Sr source.

problem in the front end chip. All tested chips showed a very good quality of the interconnections at 50 μm pitch, as well as a responding sensor. Only four channels out of more than 20 thousands showed interconnection problems.

3. Beam Test Setup

Due to beam time constraints, only three out of the five aforementioned SuperPix0 chips were tested with beam. The beam test was carried out at CERN, at the SPS H6 beam line delivering 120 GeV pions in spills lasting 9.5 s and separated by about 40 s. In the region of the experimental setup the beam was characterized by widths of about 8 and 4 mm rms on the horizontal and vertical planes, respectively. As a reference telescope six planes of 2×2 cm^2, double-sided silicon strip detector with 25 μm strip pitch on the p-side and 50 μm pitch on the n-side [**?**] were used. The readout pitch was 50 μm on both sides. Three planes were placed before the devices under test (DUT), and three after them, at distances of 3.5 cm from each other and either 25 or 35 cm from the DUTs, depending on the configuration. All detectors were placed on a custom motorized table with remote control. The reference telescope was used both to trigger events and determine the impact point of tracks at the DUT. One of the chips was used to study the dependence of the efficiency on the angle of the impinging particles, whereas either one or two chips were put in the beam line when studying the dependence of the efficiency on the value of the discriminator threshold. The schematics of both setups are shown in Fig **??**.

Figure 5: Test beam setups with either one (left) or two (right) DUTs

4. Trigger and Data Acquisition

The DAQ infrastructure is very similar to the one described in detail in [?]. The main elements are two programmable VME 9U EDRO (Event Dispatch and Read-Out) boards [? ?] organized in a master-slave configuration and responsible for programming the front end chips of both the telescope and the DUT. The master EDRO is connected to the first, third, fourth and last plane of the telescope. It generates and distributes to all elements both the readout and BCO clocks, as well as the triggers. These are based on hit multiplicity on each side of the telescope planes connected to the master. The slave is connected to the remaining planes of the telescope and to the DUT. Both EDRO boards act as event builder, packing time-ordered information from the telescope and the DUT in events that are then sent out via optical links (S-link [?]) to a Robin card [?] on a remote PC where they are written to disk. Online monitoring is performed on another PC complementing the DAQ system. The programmable BCO clock defines the time resolution of the experiment by dividing the time in corresponding events. Its period can vary from 400 ns up to 500 μm $\dot{}$For all data collected during the beam-test the BCO period was set to 5 μm $\dot{}$

The DAQ software is built on the ATLAS TDAQ software infrastructure [?], which provides a complete environment with remote process control and communication, finite-state-machine, inter-process messaging, online monitoring and histogramming as well as a textual database infrastructure for run and front end configuration. The team developed applications, plugins, configura-

tion and monitoring programs specific to our EDRO boards and information stored in the raw events.

The analysis of the BCO information stored in each event allowed the DAQ rate to be measured, together with the DAQ dead-time, over the duration of each spill. A maximum acquisition rate in the order of 40 kHz was observed. The data acquisition was dead-time free for the first half of each spill, when events could be buffered in the Robin card while waiting to be copied to disk. In the second half of each spill the DAQ rate was limited to roughly 20 kHz.

5. Collected Data Sample

Trigger utilizzato; ulteriori richieste e loro efficienza dove applicabile; statistica di tutti gli eventi utilizzati per le varie analisi/risultati e per chip (tabella?)

6. Detector Performance

6.1. Silicon Telescope Alignment and Track Reconstruction

For each event, we reconstruct tracks using the silicon telescope hits. We rely on the same track-reconstruction software that has been used for the analysis of a former test-beam [**?**]. For this analysis, the track finding algorithm has been improved to use a variable number of telescope planes, since we use now six planes whereas four were used in the past.

Triggered events typically have just one track, with one hit for each of the two sides, for each of the 6 telescope planes. We set our reference frame with the z axis along the beam, the x axis in the horizontal plane and the y axis in the vertical plane, pointing up. The p-side silicon strips measure the u detector coordinate along x, while the n-side strips measure the v detector coordinate along y. The reconstruction algorithm relies on the fact that the telescope planes have high efficiency and low noise, and that most triggered events contain just one track with all its related hits, with nothing else but a very small number of noise hits. Adjacent fired strips are grouped in clusters, and the position of each

cluster is calculated by weighting the strip positions with their measured charge. The clusters primarily consist of one or two strips, in similar proportions [**?**]. For each silicon detector, each u hit is combined with each v hit on the other side to define a space hit. All possible straight lines connecting the space-points of the two outer detectors are considered, together with the closest space-points in the intermediate detectors. The associated hits are fitted to straight lines with a minimum χ^2 fit, using roughly estimated hit uncertainties from the former data analyses [**?**].

In a first phase, we align the telescope planes using only events where a single track is reconstructed, with hits on all sides of all planes within 1 mm in the xy projection, without any requirement on the track χ^2. The beam tracks have an angular distribution that is close to normal incidence 5.0 ± 0.2 mRad in xz plane, and 0.7 ± 0.2 mRad in the yz plane. In these conditions, the data permit the alignment of the xy detector translations, and of the rotation angle around the z axis, whereas there is no significant sensitivity to align the translations along z and the rotations around x and y better that the nominal position uncertainties.

We assume that the first and the last telescope planes are positioned at their nominal position, and we align the remaining planes by minimizing the residuals of the hits with respect to the extrapolated fitted tracks. The alignment procedure is based on the measurements of the dependence of the mean residual in the u and v views both from the u and v coordinates and is described in more detail elsewhere [**?**].

After the telescope alignment, we select events with just one track, with hits on both sides of all six planes, and $P(\chi^2) \geq 10\%$. In a typical run, all these requirements correspond to an efficiency roughly around 50% of all logged events. The resulting data-set has residuals distributions (averaged over all telescope planes) which can be approximately fitted with Gaussians with mean consistent with zero and $\sigma = 5\,\mu$m and $\sigma = 9\,\mu$m in the x and y view, respectively. The p-side resolution is better because the presence of an additional floating strip improves the uniformity of the charge splitting among the readout strips.

The residual distributions of a typical run (Figure **??**) show systematic effects

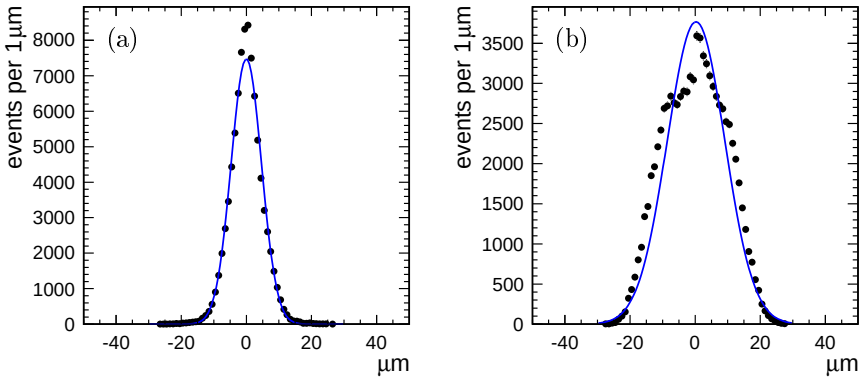

Figure 6: Example residual fit for track hits on the telescope silicon detectors, on the p-side (a) and on the n-side (b). The plots include the track fit hits residuals on all six planes combined. Because of the requirement on the track fit χ^2 probability, the residual distribution tails are truncated.

that induce sizable deviations with respect to a Gaussian distribution. We could not find evidence connecting the shapes of the residual distributions to mis-bonded channels or to the presence of insensitive strips. At any rate, the widths of the residual distributions on the telescope planes indicate that the extrapolation on the devices under test (50 μm-pitch hybrid pixels with digital readout) are precise enough for the rest of the analysis.

6.2. Hybrid Pixels Efficiency

We study the efficiency of the device under test (DUT) as a function of the angle of the track with respect to the normal to the detector (incidence angle θ), and as a function of the threshold used in the digital comparator. In different data-taking runs, the DUTs were rotated in order to change the angle from 0° to 70° with respect to normal incidence, in the xz plane, and the thresholds were varied from 730 to 820 DAC counts, corresponding to a range from about 12.5% to 40.6% of a minimum ionizing particle (m.i.p.). Relatively high thresholds were used in order to overcome data-acquisition limitations of the prototype pixel detectors under test. In the following, the plots include the result of a

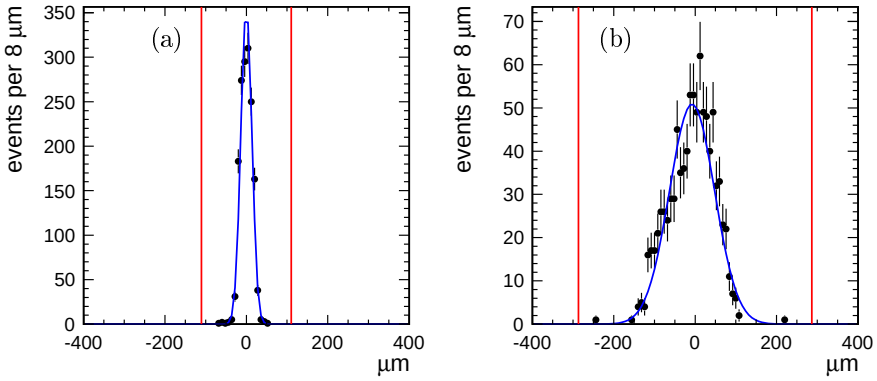

Figure 7: Example u-view residual fit for tracks hitting a hybrid pixel detector at normal incidence (a) and at 60° incidence angle (b). The residual is defined as the position of the reconstructed hit minus the extrapolated track position. The curve shows a Gaussian fit. This data was taken at a threshold corresponding to about 25% of a m.i.p.. The red vertical lines show the requirements on the residual to consider the hit associated to the extrapolated track.

coarse Monte Carlo simulation of the detector response, which is described in the next section.

Hits are defined as clusters of fired pixels that are either adjacent or separated by up to one non-fired pixel along either u or v. The cluster u (x) and v (y) positions are set to the unweighted averages of the u and v positions of the fired pixels.

To associate DUT hits to the extrapolated track, we study the residual distributions. We first align the DUT position in x and y by measuring the mean of the x and y residuals. No alignment is performed on the angle around the z axis and on the other degrees of freedom. After alignment, we observe centered and approximately Gaussian residual distributions with a negligible amount of noise hits **??**. The width of the residual distributions is driven by the DUT intrinsic resolution, which is nominally $50\,\mu\text{m}/\sqrt{12} \approx 14.4\,\mu\text{m}$ at normal incidence and increases with the incidence angle because the track ionization affects a larger number of pixels, some of which may more often be under threshold. From the geometry of $200\,\mu$m thick sensors with $50\,\mu$m pitch pixels, we expect

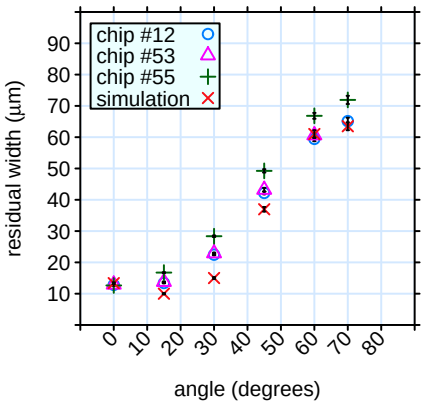

Figure 8: Dependence of the u-view residual distribution width from the track incidence angle for three pixel detectors under test. This data was taken at a threshold corresponding to about 25% of a m.i.p.. The plot also reports the result of a Monte Carlo simulation.

that tracks at 60° affect an average of 8 pixels along the x coordinate, augmenting the nominal expected intrinsic resolution to about $400\,\mu\text{m}/\sqrt{12} \approx 115\,\mu\text{m}$. Figure **??** reports the x residual width, as estimated by the σ of a Gaussian fit, as a function of the track incidence angle for the three pixel sensors under test. From $\theta = 0$ to $\theta = 70°$, the width increases approximately from $10\,\mu$m to $70\,\mu$m, while the y residual width increases from $15\,\mu$m to $19\,\mu$m. The discrepancy between the x and y residual widths at normal incidence is understood to originate from the different uncertainties of the track extrapolation in the horizontal and vertical plane, caused by the different resolution of the silicon telescope.

We associate hits to extrapolated tracks by requiring that they are closer than 4 times the (angle dependent) residual distribution width plus $60\,\mu$m to account for non-Gaussian tails caused by delta-rays. We measure the efficiency by dividing the number of events with at least one associated hit by the total number of tracks that extrapolate to the sensitive area of the DUTs. Due to fabrication defects, the prototypes are insensitive on 4 pixel columns at the center of the wafers in the u-view: this area is excluded from the sensitive area together with a safety margin corresponding to an additional $50\,\mu$m pixel spacing. To avoid border effects, we exclude from the sensitive area $50\,\mu$m from

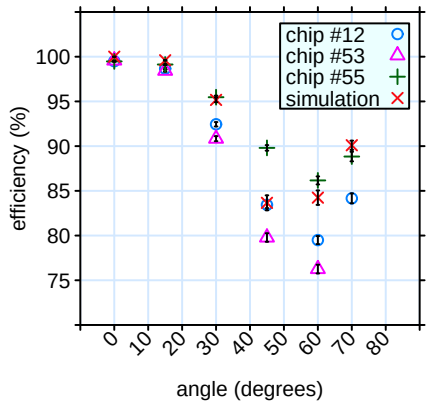

Figure 9: Hit efficiency as a function of the track incidence angle for three pixel detectors under test. This data was taken at a threshold corresponding to about 25% of a m.i.p.. The plot also reports the result of a Monte Carlo simulation.

the top and the bottom and 150 μm from the left and the right borders of the detector. We observe that the pixel detectors at non-zero track incidence are inefficient in an area where their aluminium frame intercepts the beam particles before they reach the sensors. Although the extent of the effect along the x coordinate is well described by geometrical shadowing, the mechanism that causes the observed inefficiency is not understood. As a consequence, the inefficient area related to the shadowing effect is also excluded in order to compute the efficiency. We obtain a Bayesan estimate of the efficiency and its uncertainty using a Jeffreys' prior [**?**], and we find that there is no significant deviation with respect to using the naive estimators $\epsilon = n/k$ and $\sigma^2(\epsilon) = n(n-k)/n^3$, where k denotes the number of hit-associated tracks and n the number of tracks that extrapolate to the sensitive area of the sensors. Figure **??** reports the efficiency as a function of the track incidence angle for the three pixel sensors under test, for data recorded with a threshold of 770 DAC counts, corresponding to a signal of 1/4 of a m.i.p.. Figure **??** reports the efficiency at normal incidence as a function of the threshold, which has been varied from 12.5% to 40.6% of the charge released by a m.i.p..

The inefficiency distribution is uniform across the u and v coordinates and

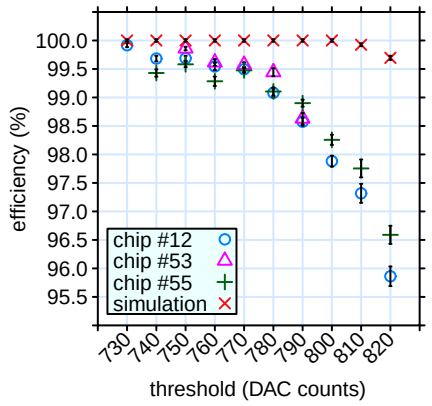

Figure 10: Hit efficiency as a function of the threshold for normal-incidence tracks on three pixel detectors under test. The DAC counts correspond to a range from 12.5% to 40.6% of the charge released by a m.i.p..

no insensitive pixel was found. We have investigated whether the inefficiency depends on the distance of the extrapolated track from the center of the pixel, finding no evidence for such hypothesis. The pixel sensors are close to full efficiency for normal-incidence tracks at the reference threshold, which corresponds to 25% of a m.i.p., but this threshold setting is not robust because we observe significant reductions of efficiency for non-zero track incidence angles and, to a minor extent, for thresholds larger than the reference one. When the track incidence angle increases, the amount of traversed silicon increases as $1/\cos\theta$ but the charge is split (along the u-view in this experimental setup) among a larger number of pixels. The data indicate that there is a sizable probability that all pixels affected by the track energy loss collect a charge below the reference threshold.

7. Hybrid Pixels Response Modeling

We have modeled the response of the detectors under test with partial success using a coarse Monte Carlo simulation, which includes the energy loss in silicon with Landau fluctuations, the charge splitting among the geometrically interested pixels, and the presence of a threshold comparator. This simple model

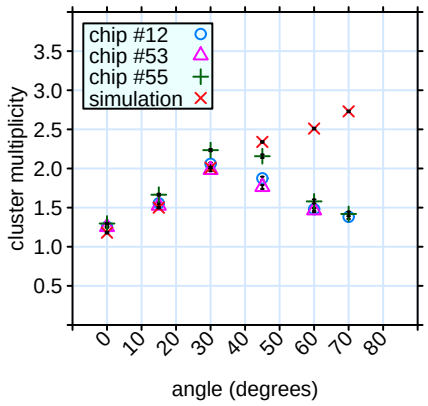

Figure 11: Hit cluster multiplicity as a function of the track incidence angle for three pixel detectors under test. This data was taken at a threshold corresponding to about 25% of a m.i.p.. The plot also reports the result of a Monte Carlo simulation.

is unable to explain the ∼0.5% "irreducible" inefficiency at low thresholds and normal incidence, which is understood as caused by the electronic readout chain dead-time, but is able to model some of the data results.

The simulation is most successful in modeling the efficiency dependence on the incidence angle (Figure **??**), where it correctly simulates both the drop for angles $\theta > 15°$ and the moderate rise from 60° to 70°. The efficiency dependence derives from the combination of two effects: the per-pixel collected charge decreases, but the number of affected pixels increases. As a consequence, the probability that *all* the pixels are under threshold first increases and then decreases.

The simulation does not appropriately simulate neither the efficiency dependence of the efficiency from the threshold (Figure **??**) nor how the number of pixels above threshold in a hit cluster varies with the track incidence angle (Figure **??**). The simulation models surprisingly well the increase of the u-view residual distribution width with the angle (Figure **??**).

8. Conclusions

The VIPIX collaboration has tested three prototype hybrid pixel detectors with 120 GeV pions at the SPS H6 beam line at CERN. A telescope consisting of six double-sided silicon strip detectors was used to reconstruct the tracks that were used to evaluate the performance of the sensors under test. The efficiency has been measured as a function of the track incidence angle and of the threshold used for the digital readout. Relatively high threshold settings were used to overcome fabrication defects that were affecting the readout chain.

From the width of the residual distributions, the detector resolution appears to be consistent with the expectation for a 50 μm pitch pixel detector with digital readout.

The pixel hit efficiency for normal incidence tracks and with a threshold corresponding to the expected energy loss of 25% of a m.i.p. has been found to be about 99.5%, apparently mainly limited by the readout chain dead-time. On the other hand, a significant efficiency drop has been observed for incidence angles larger than 15°, which is understood to be related to charge splitting among an increasing number of pixels. A coarse Monte Carlo simulation is able to partially model the features observed in the data and suggests that lowering the threshold to $\sim$13% of a m.i.p. would result in a sensor that is fully efficient at all incidence angles.

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