SVT-TDR Status

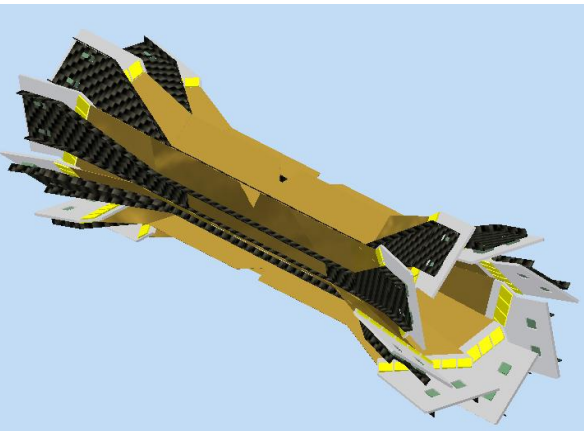
SVT-Parallel Sessions
Frascati, Dec 13- 2011
2nd SuperB Collaboration Meeting

- TDR work update
- Layer0 strategy for TDR
- TDR writing

- Giuliana Rizzo
- Universita' & INFN Pisa

SVT toward TDR

- Things are shaping up!
- Work can be completed by the end of feb.



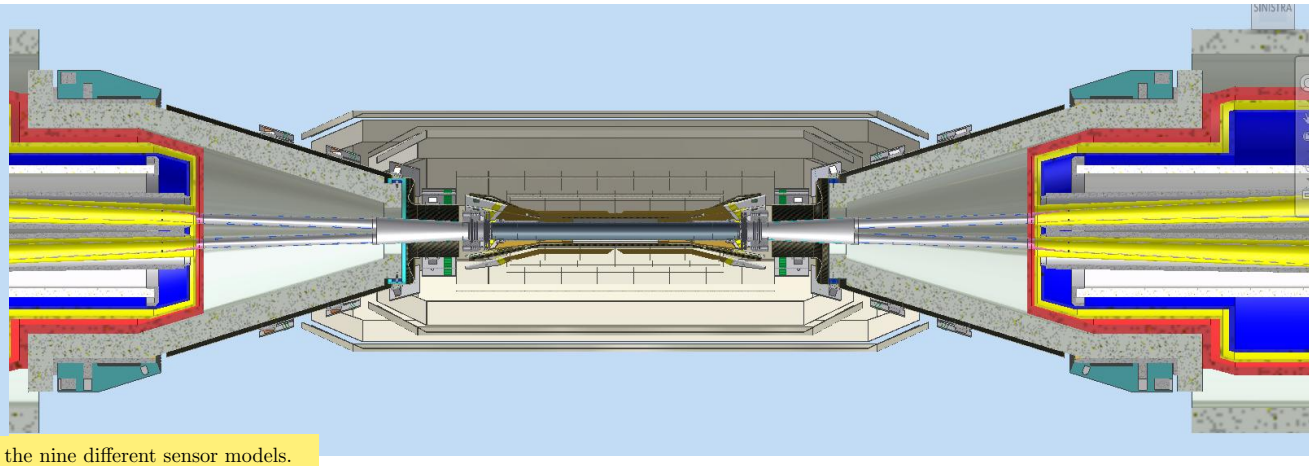
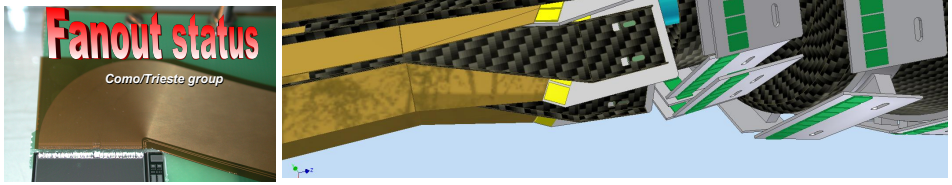


Table 6.1: Physical dimensions, number of strips and pitches for the nine different sensor models.

Sensor Type	0	I	II	III	IVa	IVb	Va	Vb	VI
Dimensions (mm)									
z Length (L)	104.0	111.7	66.5	96.4	114.5	119.9	102.2	106.0	68.0
ϕ Width (W)	13.9	41.3	49.4	71.5	52.8	52.8	52.8	52.8	52.8-43.3
Thickness	0.20	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
PN junction side reads	u	z	z	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ
Strip Pitch (μm)									
z (u for Layer 0)	50	50	50	55	105	105	105	105	105
ϕ (v for Layer 0)	50	50	55	50	50	50	50	50	50 $\rightarrow$ 41
Readout Pitch (μm)									
z (u for Layer 0)	50	100	100	110	210	210	210	210	
ϕ (v for Layer 0)	50	50	55	100	100	100	100	100	100 $\rightarrow$ 82
Number of Readout Strips									
z (u for Layer 0)	1536	1104	651	865	540	565	481	499	318
ϕ (v for Layer 0)	1536	799	874	701	512	512	512	512	512



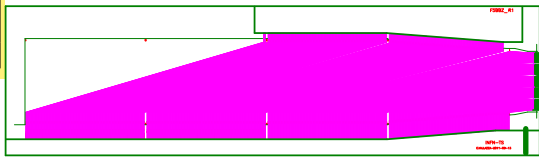
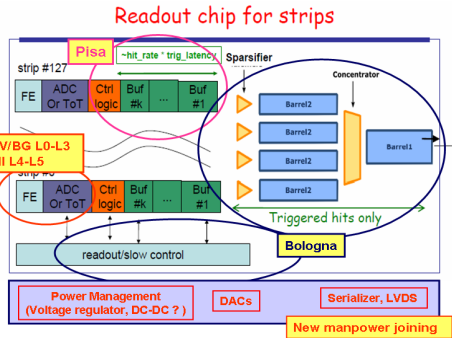
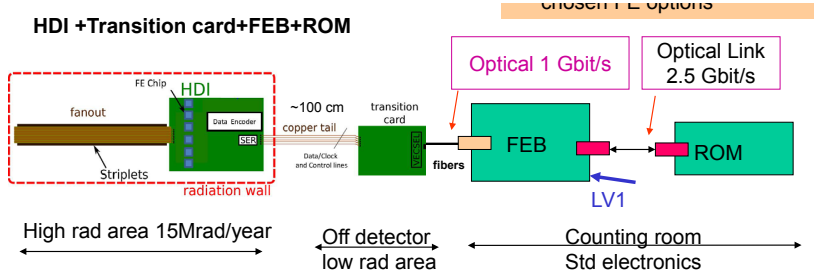


Figure 6.2: Design of a z fanout prototype.





Which Layer0 in TDR as baseline?

- Updating fastsim configurations, for striplets and hybrid pixels, with latest material budget evaluation for a fair comparison among options:
  - more realistic material for striplets (0.4→ 0.55%X0)
  - less conservative for HP (1.1→ 0.9%X0) , considering recent R&D (LHC)
- Striplets will perform anyway better without background.
- With full luminosity striplets have occupancy of 5-10% (safety factor included) depending on how aggressive can be on the time window cut applied for reconstruction (50-100 ns). More detailed study my be needed on this.

- Effect of high background on performance crucial for a decision on Layer0 technology used as baseline, but study not yet ready and timeline not clear. With these conditions wise to postpone this decision after TDR.
- In TDR can present both options (striplets and HP) as viable, even if presented with different level of details, saying that decision will be taken considering more carefully performance, readiness for the start of data, taking, etc etc
  - More advanced thinner pixel options (MAPS or thin high resistivity pixels) less mature, can be considered for a later Layer0 upgrade.
- Addendum to TDR with details on Layer0 after decision ~1 yr later?

Which Layer0 in TDR as baseline?

Present status of the 2 main Layer0 options:

Striplets

- New striplets design complex but now seems feasible.
  - FE chip has to be developed anyway as for all SVT layers
  - Layer0 rates are not an hard limit for the proposed architecture but chip complexity increase with striplets requirements.
- Quite detailed striplets design can be ready for TDR timeline (feb 2012).
- Striplets can be ready for the start of data taking (as the rest of SVT).

Hybrid Pixels

- HP still requires significant R&D to be deployed in Layer0 with 50x50 um pitch (or similar) and material budget < 1%X0.
- Detailed pixel design cannot be ready for TDR (feb 2012). It might require 2 more months after completion of other activities.
- Readiness of HP for start of data taking (???) not sure (requires specific R&D + manpower + funding).

SVT TDR Writing

- Editors produced a first draft of detailed outline (mostly in svn) and some started to write text and insert relevant tables pictures.
- First estimate of pages was 90, but will try to end up with ~60 pages.

1. Vertex Detector Overview (12) – G. Rizzo – outline
2. Backgrounds (4) – R. Cenci outline
3. Detector Performance Studies (6) – N. Neri - outline + description of content
4. Silicon Sensors (8) – L. Bosisio outline + some text and tables
5. Fanout Circuits (8) – L. Vitale-M. Prest outline + some text and tables
6. Electronics Readout (28)
    1. Readout Chips (10) – V. Re outline + most of text and tables (doc file!)
    2. Hybrid Design (10) – M. Citterio outline
    3. Data Transmission (8)– M. Citterio outline
    4. Power Supplies (1??) -???

    SVT DAQ (M. Villa) will be in the ETD section
7. Mechanical Support & Assembly (14) – S. Bettarini/F. Bosi outline + description of content
8. Layer0 pixel upgrade options (10) – G. Rizzo/L. Ratti+others outline + some text
9. Services, Utilities (2) -?? outline

SVT TDR Writing

~ 10 pages in svn + 10 in doc file..

TDR writing has started but work in some area will continue until end of feb 2012.