Analog Section for the Silicon Strip Detectors of the Super B SVT Inner Layers

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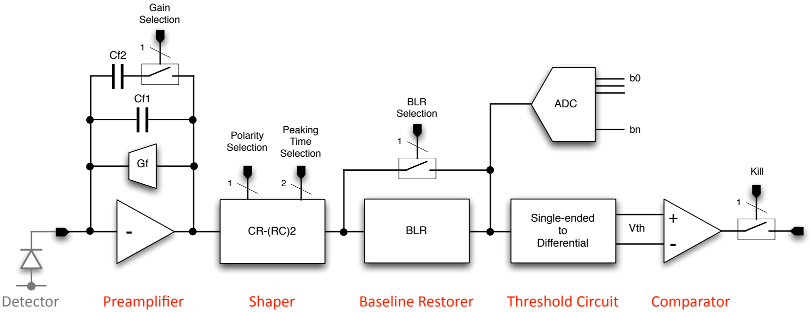
Electronic Readout for SVT Inner Layers (L0-L3)

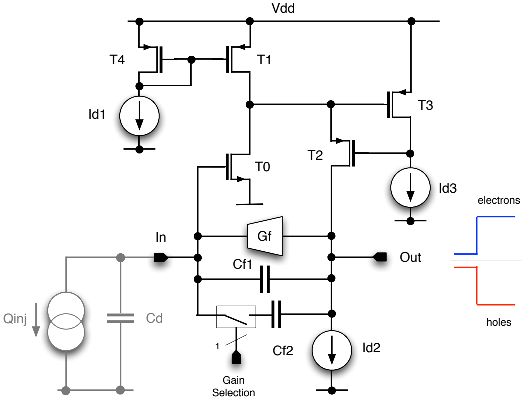
- Microstrips and striplets detectors are the baseline option for the design of the SVT fast (Layers 0 to 3) front-end at SuperB
- ASIC: the signals from the silicon strip detectors will be processed by a custom-designed IC based on a 130 nm planar technology with 128 channels
- Analog Channel
  - amplification
  - filtering
  - threshold discrimination
  - 3-4 bit analog information about the signal amplitude
- Main requirements
  - Operating temperature: $<40\ ^\circ$C
  - Radiation tolerance: >3 Mrad/year for 10 years
  - Power dissipation: <4 mW/channel
  - Signal polarity: readout channel should be capable of reading signals from both P and N-side of the strip detectors
  - Dynamic range: 10-15 MIP charge
  - Analog Resolution: 0.2 MIP minimum input charge
  - Hit efficiency: $>95\%$ at design luminosity
  - Peaking Time: ≤ 25 ns for Layer 0
  - Signal-to-Noise Ratio: >20
  - Threshold dispersion: <300 e- rms
- Simulation results for a preliminary version of the charge preamplifier and the shaping stage of the SVT inner layers will be shown

Analog channel block diagram



The analog channel consists of

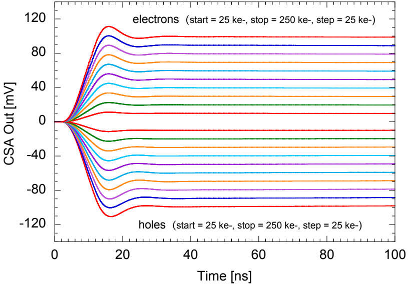
- Charge-sensitive preamplifier with gain selection (1 bit)
- Unipolar semi-Gaussian shaper with polarity (1 bit) and peaking time (2 bit) selection options
- Symmetric baseline restorer to achieve baseline shift suppression, may be included or not (1 bit)
- Hit discriminator threshold circuit and comparator
- 3-4 bit analog-to-digital conversion will be performed by a Flash ADC or by means of a Time-Over-Threshold (TOT) detection

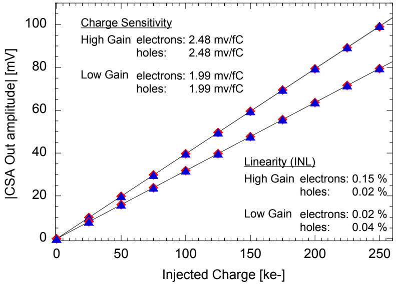


Main design features	
Chip Bias V_{DD}	1.2 V
PA input W/L	2000/0.2
PA input I_D	500 μA
Power consumption	1.1 mW
Feedback C_{f1}, C_{f2}	400 fF 100 fF
Reset G_f	100 nS

- Architecture: active folded cascode (with local feedback) loaded by an active cascoded load
- Sensitivity: low gain 2.0 mV/fC ($C_f = C_{f1} + C_{f2}$), high gain 2.5 mV/fC ($C_f = C_{f1}$)
- Reset: performed by a time continuous feedback network implemented with a differential pair ($\tau \approx 5$ μs at low gain and ≈ 4 μs at high gain)

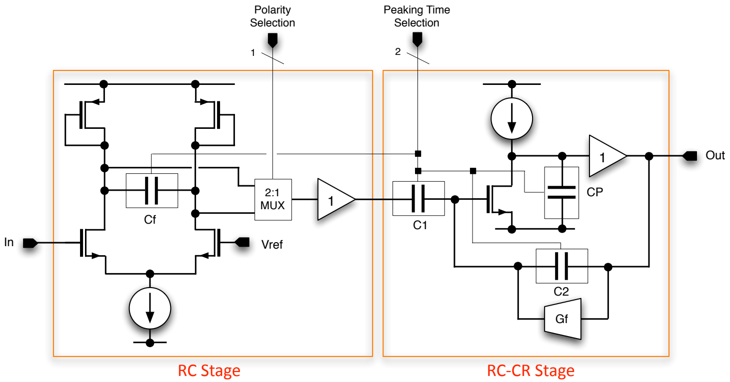
CSA response and dynamic range





- Rise time: t_r=7 ns for both holes and electrons
- Charge sensitivity: low gain 1.99 mV/fC (electrons and holes), high gain 2.48 mV/fC (electrons and holes)
- Dynamic range: the CSA covers the full dynamic range of 15 MIP (240 ke- in L0) for both the input signal polarities and gain settings
- Linearity: $<$0.2 %

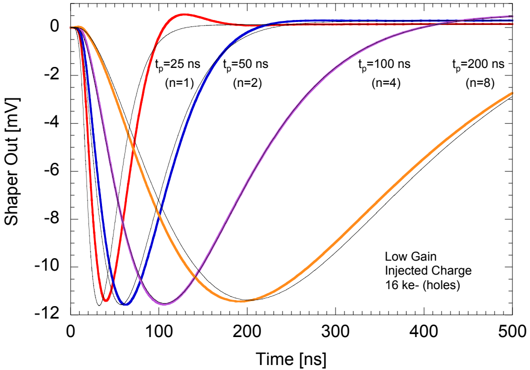
Shaping circuit



- Shaping function: Unipolar semi-Gaussian (RC^2-CR)
- Polarity selection (1 bit): allows to operate with signals delivered both from n- and p- sides of double-sided strip detectors
- Peking time selection (2 bit): obtained by setting the values of capacitances in the shaper according to the following relationships (with t_{P0}=25 ns, $C0$=50 fF and n=1,2,4,8):

$$
\begin{aligned}
t_P &= n \cdot t_{P0} \\
C_P &= n \cdot C0 \\
C_1 &= n \cdot 4 \cdot C0 \\
C_2 &= n \cdot 2 \cdot C0 \\
C_f &= n \cdot 2.5 \cdot C0
\end{aligned}
$$

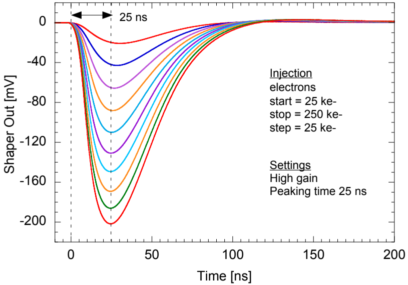
Peaking Time Selection

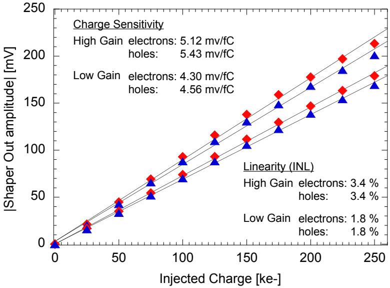


	Peaking Time [ns]	
n	Nominal	Simulated
1	25	30
2	50	55
4	100	100
8	200	190

- Good agreement between ideal (black lines) and simulated (colored lines) shaping functions and peaking times
- A better matching can be obtained with a fine tuning of the shaping circuit capacitances (to be done)

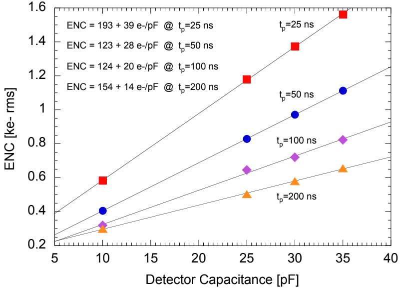
Shaper Output response and dynamic range

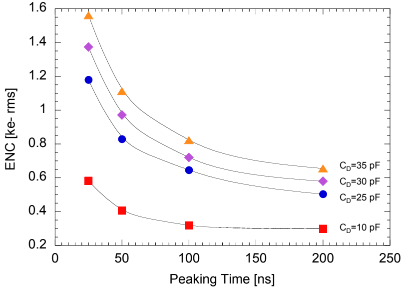




- Charge sensitivity: low gain ≈4.5 mV/fC (electrons and holes), high gain ≈5.5 mV/fC (electrons and holes)
- Dynamic range: the shaper covers the full dynamic range of 15 MIP (240 ke- in L0) for both the input signal polarities and gain settings
- Linearity: worst in high gain setting (≈3.5 %) with respect to low gain setting (≈2 %)

Equivalent Noise Charge

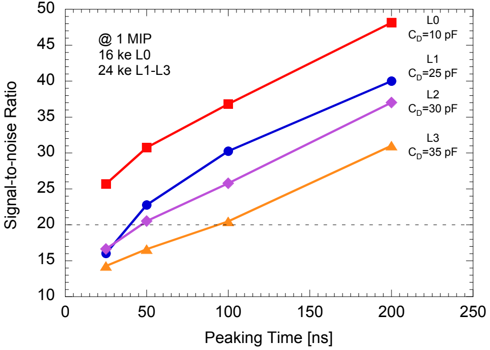




Layer	C_D [pF]	t_p [ns]	ENC R_S [e rms]	ENC CSA [e rms]	S/N (1 MIP)
0	10	25	220	580	26
1	25	100	460	650	30
2	30	100	590	720	26
3	35	200	410	660	31

S/N $>$20 for all the layers (1 MIP is 16 ke- in L0 and 24 ke- in L1 to L3)

S/N ratio vs t_P at 1 MIP



- L1 and L2: S/N remains >20 moving from the foreseen peking time of 100 ns to 50 ns
- L3: S/N remains >20 moving from 200 ns to 100 ns

Conclusions

- Simulation of the charge preamplifier and the shaping stage of the SVT inner layers almost complete
- Power consumption <4 mW/channel
- Charge sensitivity: adjust the low gain to best fit the 2/3 ratio as for the charge delivered by sensors belonging to different layers
- Threshold adjustment at strip level could be necessary due to the low value of charge sensitivity
- Good performance in terms of noise (S/N$>$20 for all layers)
- In next weeks the design of the remaining blocks (BLR and threshold discriminator) will be also completed in order to have a preliminary version of the channel ready for the TDR

Backup Slides

Microstrip detector: proposed layer grouping

<table>
<tr><th>Layer</th><th>C_D [pF]</th><th>available t_p [ns]</th><th>selected t_p [ns]</th><th>ENC from R_S [e rms]</th><th>ENC [e rms]</th><th>Channel width [μm]</th><th>Hit rate/ strip [kHz]</th><th>Efficiency 1/(1+N)</th></tr>
<tr><td>0</td><td>11.2</td><td rowspan="4">25, 50, 100, 200</td><td>25</td><td>220</td><td>740</td><td rowspan="4">3000</td><td>2060</td><td>0.890</td></tr>
<tr><td>1</td><td>26.7</td><td>100</td><td>460</td><td>940</td><td>697</td><td>0.857</td></tr>
<tr><td>2</td><td>31.2</td><td>100</td><td>590</td><td>1100</td><td>422</td><td>0.908</td></tr>
<tr><td>3</td><td>34.4</td><td>200</td><td>410</td><td>940</td><td>325</td><td>0.865</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">52.6</td><td rowspan="4">400, 600, 800, 1000 (or 500 and 1000)</td><td>500</td><td>490</td><td>1000</td><td rowspan="4">9000</td><td rowspan="2">47</td><td>0.947</td></tr>
<tr><td>600</td><td>440</td><td>940</td><td>0.937</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">67.5</td><td>800</td><td>560</td><td>1090</td><td rowspan="2">28</td><td>0.949</td></tr>
<tr><td>1000</td><td>500</td><td>1030</td><td>0.937</td></tr>
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